7.1 An 8b Source Driver for 2.0 inch Full-Color Active-Matrix OLEDs Made with LTPS TFTs

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Six bit RGB digital interface source drivers made with LTPS TFTs have previously been successfully developed for mobile displays [1-2]. But 8b source drivers are now required in the mobile display market for high image quality. There are many challenges to integrating 8b source drivers using LTPS TFTs because of the high value of, and large variations in, the threshold voltage. Also, the minimum feature sizes in LTPS TFT processes are roughly 20× larger than in modern LSI technologies [3]. We present here an LTPS TFT-based source driver with an 8b DAC that can be integrated in a small and narrow area for 2.0 inch QVGA AMOLED displays.

Normally, the area of an individual pixel in a 2.0 inch QVGA display is only 42μm×126μm. For this narrow pitch we applied three technologies to integrate an 8b source driver. First, we use a new source driver structure. As shown in Fig. 7.1.1, it has , from top down, a top 4b DAC(D7[MSB], D6, D5, D0[LSB]), a level shifter block, a S/H block, a shift register, another S/H block, another level shifter block, a bottom 4b DAC(D4, D3, D2, D1) and a one-to-three DEMUX. Using this structure reduces the 8b source-driver area by 40% compared to a conventional source driver.

Second, a new 8b DAC circuit is used with the 1:3 DEMUX. Fig. 7.1.2 shows the equivalent circuit of the 8b DAC. As shown, the top 4b decoder selects two neighboring nodes from the 9 reference voltages. Then, two pairs of reference voltages are created by the voltage drops across the reference selection switches. One reference voltage pair is for an odd gray level and the other is for an even gray level. The odd reference voltage pair is given by Equations (1) and (2). The even reference voltage pair can be calculated by the same methods.

$$V_{Odd\_High} = HRV - (Ra \text{ or } Rb) \times I \tag{1}$$

$$V_{Odd\_Low} = HRV - \{(Ra \text{ or } Rb) + (Rf \text{ or } Re) + r_{Total}\} \times I \tag{2}$$

$$I = \frac{HRV - LRV}{\{(Ra \text{ or } Rb) + (Rf \text{ or } Re) + r_{Total} + (Rc \text{ or } Rd)\}} \tag{3}$$

where, *Ra*, *Rb*, *Rc*, *Rd*, *Re* and *Rf* are the on-resistances of MP1, MP2, MP3, MP4, MP5 and MP6, respectively, *Ra = Rd, Rf = Re, Rb = Rc,* $r_{Total} = r1 + r2 + r3 = 320k\Omega$, and r_{Total} is implemented by a poly-silicon layer.

The resistance of the poly-silicon layer should be chosen to minimize horizontal crosstalk that is caused by the reference voltage drop on the horizontal metal line routing. Therefore, we simulated the optimum total resistance in each DAC with the worst-case condition, which is when 90% of all DACs in the source driver circuits select the same reference voltage. We then find the minimum input resistance of a DAC required to reduce the crosstalk level to less than 1 gray level with our target panel specification in spite of ±20% poly resistance variation. On the other hand, the bottom 4b decoder divides the resistance string. That is, the data voltage level is set by the ratio of resistance values between two selected reference voltage sources. As shown in Fig. 7.1.2, we can obtain 4 different voltage levels with the 4 combinations of top and bottom 4b decoders. The data voltage of the 1st gray level is given by Equation (4). The data voltages of the other three gray levels can be calculated in similar fashion.

$$V_{1st\_gray} = (V_{Odd\_High} - V_{Odd\_Low}) \times \left(\frac{Rf + r1}{Rf + r_{Total}}\right) + V_{Odd\_Low} \tag{4}$$

Also, the other 28 gray values can be calculated by ratios of different switch on resistances and poly-resistor values. Since there are 9 reference voltage levels and 32 gray values between two neighboring reference voltage levels, a total of 256 gray levels can be obtained.

Lastly, we also applied a pre-charging method to overcome the insufficient data line charging period, which is only one third of normal driving time due to the 1:3 DEMUX. Figure 7.1.3 shows the circuit simulation results for the 8b DAC using pre-charging. The first 3μs are used for the pre-charge operation, which charges the high reference voltage level between the two neighboring nodes selected by the top 4b decoder. During the last 7μs the capacitor at the nodes will discharge and keep the actual data. We have achieved a data charging error less than 0.0025LSB even though the charging time of the data-line capacitor was reduced to 1/3 of the normal time.

While designing this DAC, typical TFT characteristics were used for the simulations. Typical N-TFT threshold voltage and mobility values are 1.15V and 100cm²/Vs, respectively, and the variation in the threshold voltage is ±0.5V. Similarly, the P-TFT threshold voltage is -1.56V with ±0.5V variation and the mobility is 80cm²/Vs. Figure 7.1.4 shows the simulation results for the 8b D/A INL and DNL. The simulated INL and DNL are less than ±1LSB even though the variations in poly-resistance and threshold voltages are ±20% and ±0.5V respectively.

Figure 7.1.5 shows ideal and measured RGB luminance from 0 to 255 gray levels with a gamma value of 2.2. The output linearity of the source driver was calculated from the luminance of each RGB pixel in the 2.0 inch AMOLED panel. Using this calculation method, Fig 7.1.6 shows the measured DNL of RGB pixel luminance obtained from Fig. 7.1.5. As shown in Fig. 7.1.6, the maximum DNL is under 1LSB even though minimum gray step voltage is 4mV.

We measured the TFT characteristics of the fabricated 2.0 inch AMOLED panel. The measured threshold voltage and mobility of the N-TFT are 1.33V and 100cm²/Vs, respectively. The threshold voltage and mobility of the P-TFT are –1.28V and 90cm²/Vs, respectively. Also, the standard deviation of the threshold voltage variations for the N-TFTs and P-TFTs are 0.26V and 0.3V, respectively. All measured results for TFT characteristics are better than were used for the simulations for the 8b DAC design.

Figure 7.1.7 is a micrograph of the fully integrated 8b source driver to operate a 2.0 inch QVGA AMOLED panel. We have used a 2μm line width and space LTPS TFT process. The heights of the DAC and digital logic part in the source driver are 2mm and 1mm, respectively. Photographs of the 8b AMOLED panel are shown in Fig. 7.1.8. The panel demonstrates 256 gray levels without line-to-line non-uniformity as expected in spite of the electrical characteristic variations of the LTPS TFTs.

We have developed an LTPS TFT-based 8b source driver for 2.0 inch QVGA AMOLED panels. This driver includes the 8b DACs using a top 4b DAC and a bottom 4b DAC structure in order to reduce the source driver size. This scheme reduces source driver size by 40% compared with a conventional source driver scheme. To overcome the driving speed, we applied an optimized pre-charging method. The experimental results show that the fabricated AMOLED panel with the 8b source driver circuit can display 16M colors successfully.

References:

[1] Y. Matsueda, R. Kakkad, and Y. S. Park "2.5-in AMOLED with Integrated 6-bit Gamma Compensated Digital Data Driver," *SID'04 Digest*, pp 1116-1119, May 2004.
[2] Y. Matsueda,. Y. S. Park, and S. M Choi "6-bit AMOLED with RGB Adjustable Gamma Compensation LTPS TFT Circuit," *SID'05 Digest*, pp 1352-1356, May 2005.
[3] Y.–C. Sung, et al., "10bit Source Driver with Resistor-Resistor-String Digital to Analog Converter," *SID'05 Digest*, Vol. 36, pp. 1099-1101, May 2005.

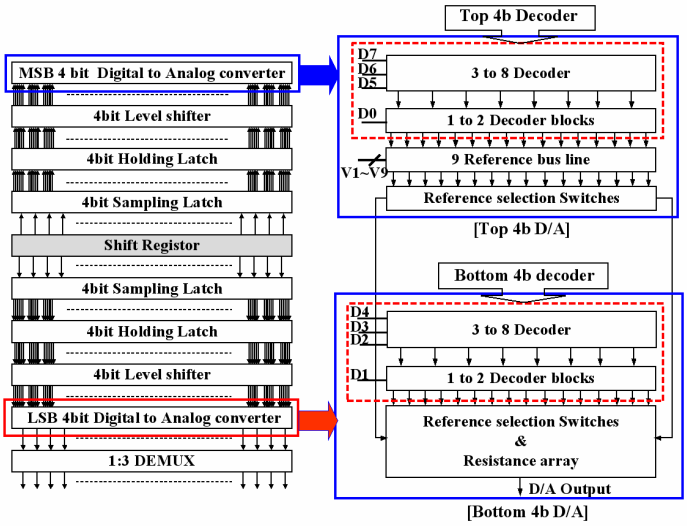

Figure 7.1.1. 8b Source driver and D/A converter structure.

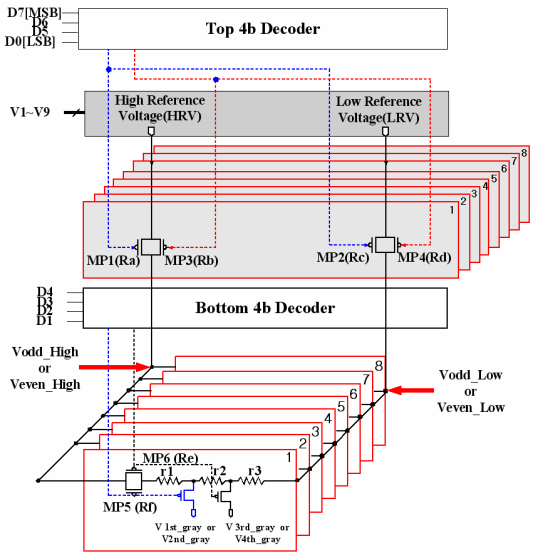

Figure 7.1.2. Equivalent circuit of 8b D/A converter.

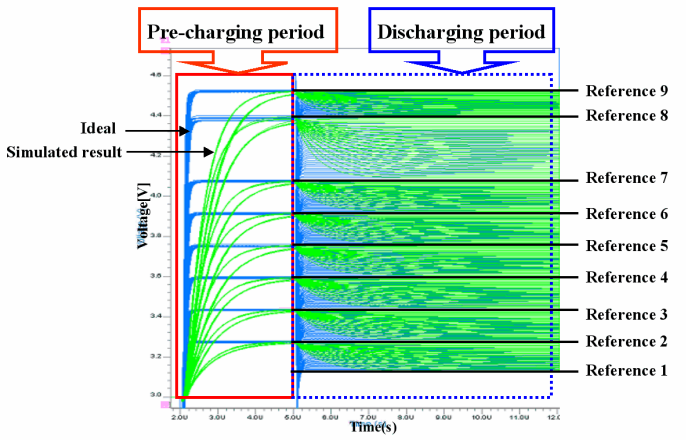

Figure 7.1.3. Charging error of 8b D/A converter.

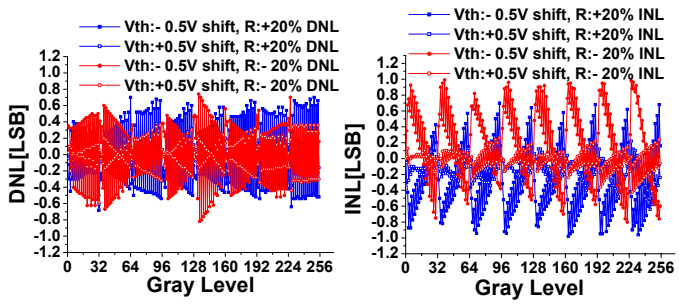

Figure 7.1.4. Simulated INL & DNL of 8b D/A converter.

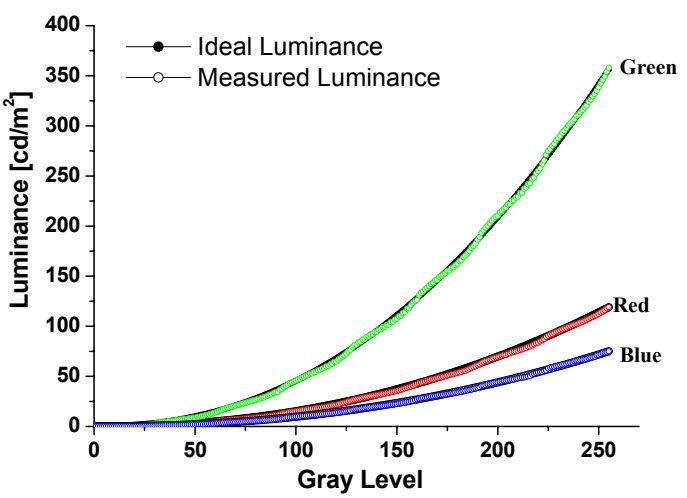

Figure 7.1.5. Measured luminance curve with gamma value of 2.2.

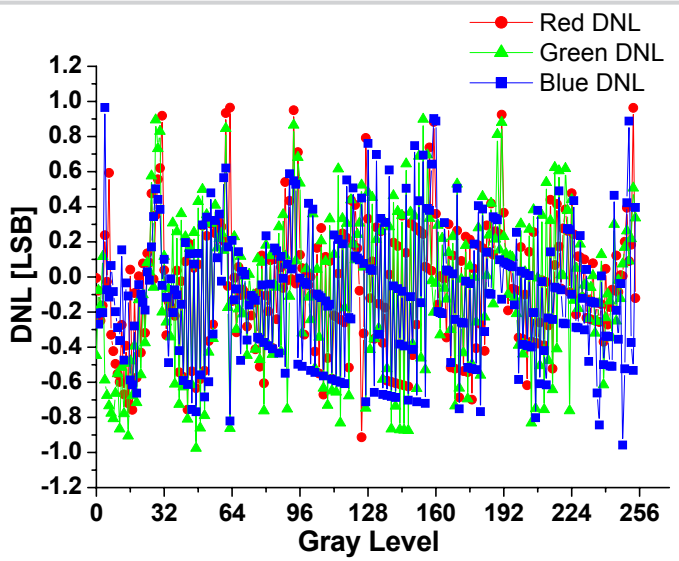

Figure 7.1.6. Measured DNL of 8b D/A converter.

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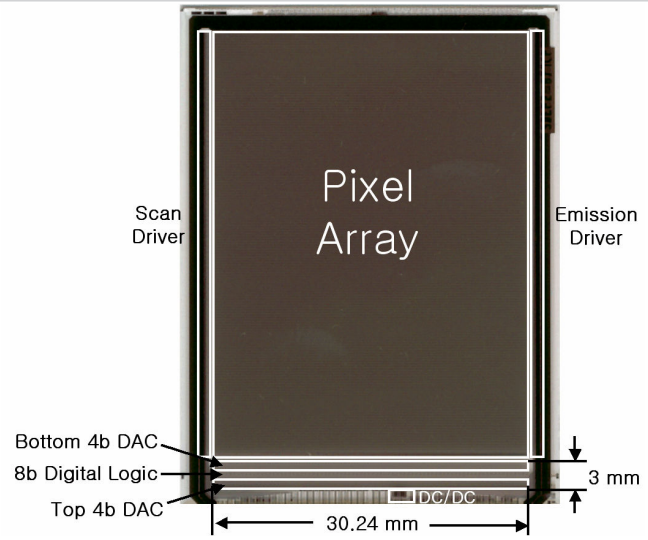

Figure 7.1.7. Micrograph of the 2.0 inch QVGA AMOLED backplane with 8b source driver, gate driver, emission driver, and DC-DC converter.

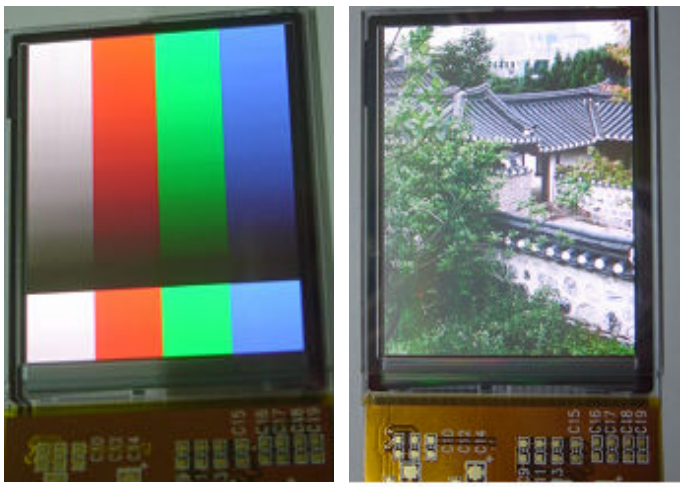

Figure 7.1.8. Photographs of AMOLED Module.

